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12EC021

M.Tech. Degree Examination, February 2013

CMOS VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Derive an expression for the drain current of an nMOS enhancement mode FET. Draw the output characteristics and mark regions of operation. **(08 Marks)**

b. Explain the following second order effects:
i) Body effect ii) FN tunneling iii) Hot electron effect **(12 Marks)**

2 a. Using output characteristics, explain the working of a CMOS inverter. What is the effect of β_n/β_p ratio on the output characteristics? **(08 Marks)**

b. Draw the small signal AC equivalent circuit of a MOSFET and obtain expressions for output conductance and transconductance in linear and saturation region. **(06 Marks)**

c. Draw the circuit diagram of a BiCMOS inverter which provides true one and true zero as outputs and explain its working. **(06 Marks)**

3 a. Draw the sketches of the process steps involved in p well CMOS fabrication and list out the masks used. **(08 Marks)**

b. Draw sketches of MOS layers and transistors using λ based design rules. **(06 Marks)**

c. Using combined voltages and scaling method. Obtain scaling factors for:
i) Number of gates ii) Channel resistance iii) Power dissipation/gate. **(06 Marks)**

4 a. Show that the inverter pair delay is invariant. **(06 Marks)**

b. What are the issues to be considered while driving large capacitive loads? Derive an expression for the width factor and number of stages when a chain of inverters is used to drive a large capacitive load so their the delay through the chain is minimum. **(08 Marks)**

c. A particular section of layout includes a 3λ wide metal path which crosses a 2λ wide polysilicon path at right angles. Assuming that the layers are separated by 0.5 μm thick layer of SiO_2, find the capacitance between the layers. The polysilicon layer in turn crosses a 4λwide diffusion line at right angles to form a transistor. Find the gate to channel capacitance. Compare it with the metal to poly capacitance already computed. Assume 2λ = 5 μm, relative permittivity of SiO_2 = 3.9, gate to channel capacitance for 5 μm technology = 4×10^{-4} pF/μm^2. **(06 Marks)**

5 a. Derive expressions for V_{OL} and V_{OH} in the case of an nMOS NOR2 gate. **(08 Marks)**

b. Explain the working of a CMOS TG in terns of its output voltage. **(06 Marks)**

c. Draw circuit diagrams of two input MUX and XOR gate with minimum transistors using TGs. **(06 Marks)**

6 a. Show that the maximum output voltage of a pass transistor is restricted to V_{DD}-V_{th} when the input and gate voltages are VDD. Give physical reason for the same. **(10 Marks)**

b. Bring out the differences between ratioed and ratioless three stage dynamic shift registers. What is the reason for such a nomenclature? **(10 Marks)**

7 a. List out the differences between combinational and sequential circuits. **(06 Marks)**

b. Discuss the general principles of band gap reference and obtain an expression for V_{BE}. **(08 Marks)**

c. What is the basic drawback of a CMOS dynamic circuit? How it is overcome in the case of a CMOS domino circuit? **(06 Marks)**

8 a. What is latch up? Suggest remedies to overcome the same. **(08 Marks)**

b. Draw circuit diagrams of NAND2 and NOR2 gates, using CMOS. **(06 Marks)**

c. Describe clock generation and clock distribution techniques. **(06 Marks)**

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